REMARKS

This response is made to the Official Action dated April 10, 2002. At the time the Office Action was mailed, claims 1, 3-17, 19-33 and 35-63 were pending. Independent claims 1, 15, 33, 47 and 54 have been amended to set forth the subject matter of the invention more clearly. Reconsideration of the application as amended is respectfully requested.

Rejections Under 35 U.S.C. § 102

The Examiner rejected claims 1, 13-17, 29-33, 45-47 and 53-54 under 35 U.S.C. § 102(e) as being anticipated by Moden et al. (U.S. Patent No. 6,297,960 B1). With specific regard to the independent claims, the Examiner stated:

> As to claim 1, Moden et al. discloses a system (Fig. 1) which *inherently* comprising a processor; and a memory device (10) *inherently* operatively coupled to the processor [it should be noted that a computer *inherently* has a processor which is coupled to a memory device for performing electrical functions], the memory device (10) comprising a plurality of vertically stacked ball grid arrays (106), each ball grid array (106) having a memory chip (102), and wherein the vertically stacked ball grid arrays comprise: a plurality of packages (104), each of the plurality of packages (104) comprising a plurality of mateable alignment features (see Fig. 9, elements 152, 154 & 156), and wherein each of the plurality of packages (104) is physically coupled to another of the plurality of packages (104)(see Fig. 9); and a plurality of memory chips (102), each of the plurality of memory chips (102) physically coupled to a respective one of the plurality of packages (104).
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> As to claim 15, Moden et al. discloses a memory board (Fig. 1) comprising a substrate (12); and a memory device (10) operatively coupled to the substrate (12), the memory device (10) comprising a plurality of vertically stacked ball grid arrays (106), each ball grid array having a memory chip (102), and wherein the vertically stacked ball grid arrays comprise: a plurality of packages (104), each of the plurality of packages (104) comprising a plurality of mateable alignment features (see Fig. 9, elements 152, 154, 156), and wherein each of the plurality of packages (Fig. 9,

element 104) is physically coupled to another of the plurality of packages (104); and a plurality of memory chips (102), each of the plurality of memory chips (102) coupled to a respective one of the plurality of packages (104) (see Fig. 9).

Claim 33 recites limitations similar to claim 15. Therefore it is rejected for the same reasons.

As to claim 47, Moden et al. discloses a device (Fig. 1) comprising a chip (102); and a package (104) operatively coupled to the chip (102), the package 104 comprising: a first side; a second side; a plurality of first mateable alignment features (see Fig. 9, element 152) on the first side of the package; and a plurality of second mateable alignment features (154, 156) on the second side of the package.

As to claim 53, Moden et al. discloses a package (Fig. 1, element 104) comprising: a first side; a second side; a plurality of first mateable alignment features (Fig. 1, element 152) on the first side of the package; and a plurality of second mateable alignment features (154, 156) on the second side of the package.

Applicants respectfully traverse this rejection. Anticipation under section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under section 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited references, the reference does not anticipate the claimed invention.

Each of the independent claims 1, 15, 33, 47 and 54 recites, in relevant part, a package comprising a plurality of non-metal mateable alignment features. It is clear from

the present specification that the alignment features are structural appendages protruding from or receding into the surface of each package that are formed to mate with alignment features on adjacent packages. The alignment features facilitate stacking the packages in a stable manner and ensure that each package is aligned with respect to each adjacent package. The alignment features are also used to support the weight of the package during reflow of the solder balls. Finally, the alignment features are used to orient the package about an axis which is perpendicular to the package. (Page 8, lines 12-18).

Conversely, the Moden et al. reference does not disclose non-metal mateable alignment features. Moden et al. discloses a metal heat transfer member 150. "The heat transfer member 150 comprises a member of suitable *metal* having downwardly extending retention T-shaped flanges 152, upon a portion of which a substrate 104 sits, and upwardly extending L-shaped members 154, the upper portion 156 serving as support for the assembly 100 located thereabove having a heat transfer member 150 located therearound." It is clear that the components of the heat transfer member 150 are necessarily metal since the Moden et al. reference is explicitly directed to "an apparatus and method for providing heat sinks or heat spreaders for stacked semiconductor devices." Col. 1, lines 12-14. To be sure, the Moden et al. reference explicitly identifies a need for the cooling of semiconductor devices on substrates where the substrates and devices are vertically stacked, and explicitly discloses that with such an arrangement the dissipation of the heat from the semiconductor devices is of concern. Col. 2, lines 33-37. Accordingly, the components of the heat transfer member 150, as disclosed, are necessarily metal to provide the stated heat dissipation. With the recitation of non-metal mateable alignment features, as set forth in the amended claims, it

should be clear that the Moden et al. reference does not recite all of the limitations and elements of the claimed subject matter.

In view of the remarks and amendments set forth above, Applicants respectfully submit that the subject matter of claims 1, 13-17, 29-33, 45-47 and 53-54 is not anticipated by Moden et al. since the present claims clearly recite elements not found in the recited reference. Accordingly, Applicants request withdrawal of the Examiner's rejection and allowance of claims 1, 13-17, 29-33, 45-47 and 53-54

Rejections Under 35 U.S.C. § 103

The Examiner rejected claims 3-12, 19-28, 35-44, 48-52 and 55-63 under 35 U.S.C. § 103(a) as being unpatentable over Moden et al. in view of Mostafazadeh et al. (U.S. Patent No. 5,783,870). The Examiner's rejections are too lengthy to be reproduced efficiently herein. However, Applicants respectfully traverse this rejection.

Applicants respectfully submit that the Moden et al. reference does not qualify as prior art against the above-referenced application under 35 U.S.C. § 103. In accordance with 35 U.S.C. § 103(c) and Pub. L. 106-113, section 4807, enacted November 29, 1999, subject matter developed by another person which qualifies as prior art only under sub-section (e) of 35 U.S.C. § 102, shall not preclude patentability where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. Here, both the Moden et al. reference and the claimed invention were, at the time the invention was made, owned by the present

assignee (Micron) or subject to an obligation of assignment to the present assignee. Since the present application was filed after November 29, 1999 and the Moden et al. reference did not issue until after the filing date of the present application, it is clear that the Moden et al. reference does not qualify as prior art under 35 U.S.C. § 102(e)/103(c). Without the Moden et al. reference, the Examiner's rejections under 35 U.S.C. § 103 are moot, since it is clear that the Mostafazadeh et al. reference alone does not disclose non-metal mateable alignment features.

In view of the remarks and amendments set forth above, Applicants respectfully submit that the subject matter of claims 3-12, 19-28, 35-44, 48-52 and 55-63 is not obvious in light of the art of record. Accordingly, Applicants request withdrawal of the Examiner's rejection and allowance of claims 3-12, 19-28, 35-44, 48-52 and 55-63.

Attachment

Attached hereto is a clean version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**CLEAN VERSION TO SHOW CHANGES MADE.**"

Conclusion

In view of the remarks and amendments set forth above, Applicants respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1, 3-17, 19-33 and 35-63. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

General Authorization for Extensions of Time

In accordance with 37 C.F.R. § 1.136, Applicants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefor. Furthermore, Applicants authorize the Commissioner to charge the appropriate fee for any extension of time to Deposit Account No. 13-3092; Order No. MICS:0038 (99-0525).

Respectfully submitted,

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CLEAN VERSION TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 1, 15, 33, 47, and 54 as set forth below:

1 (twice amended). A system comprising:

a processor; and

a memory device operatively coupled to the processor, the memory device comprising a plurality of vertically stacked ball grid arrays, each ball grid array having a memory chip, and wherein the vertically stacked ball grid arrays comprise:

a plurality of packages, each of the plurality of packages comprising a plurality of non-metal mateable alignment features, and wherein each of the plurality of packages is physically coupled to another of the plurality of packages; and

a plurality of memory chips, each of the plurality of memory chips physically coupled to a respective one of the plurality of packages.

15 (twice amended). A memory board comprising:

a substrate; and

a memory device operatively coupled to the substrate, the memory device comprising a plurality of vertically stacked ball grid arrays, each ball grid array having a memory chip, and wherein the vertically stacked ball grid arrays comprise:

a plurality of packages, each of the plurality of packages comprising a plurality of non-metal mateable alignment features, and wherein each of the plurality of packages is physically coupled to another of the plurality of packages; and

a plurality of memory chips, each of the plurality of memory chips coupled to a respective one of the plurality of packages.

33 (twice amended). A stacked ball grid array comprising:

a plurality of packages, each of the plurality of packages comprising a plurality of non-metal mateable alignment features, and each of the plurality of packages coupled to another of the plurality of packages; and

B3 (cancl'd)

a plurality of memory chips, each of the plurality of memory chips coupled to a respective one of the plurality of packages.

47 (twice amended). A device comprising:

a chip; and

a package operatively coupled to the chip, the package comprising:

B4

a first side;

a second side;

a plurality of first non-metal mateable alignment features on the first side of the package; and

a plurality of second non-metal mateable alignment features on the second side of the package.

B5

54 (twice amended). A package comprising:

a first side;

a second side;

a plurality of first non-metal mateable alignment features on the first side of the package; and

a plurality of second non-metal mateable alignment features on the second side of the package.